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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,436	12/05/2003	Yung-Tin Chen	MA-111	9395

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EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,436	CHEN, YUNG-TIN	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-75* is/are pending in the application.

4a) Of the above claim(s) *1-67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *68-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Applicant's election without traverse of Group III (claims 68-75) in the reply filed on 12/02/05 is acknowledged.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 68-71 are rejected under 35 U.S.C. 102(e) as being anticipated by Fritze et al. (6,934,007).

Fritze et al. teach a method of forming a feature pattern on a substrate, comprising: (a) exposing the substrate, using a mask having a pattern of features thereon, with X-dipole illumination, to produce a dense feature illumination pattern on the substrate; (b) exposing the substrate, using the same mask having the pattern of features thereon, with Y-dipole illumination, to produce a dense feature illumination pattern on the substrate; and (c) exposing the substrate to trim portions of the pattern on the substrate.

And wherein the pattern of features is a template pattern of regular dense features.

And wherein the pattern of features is a template pattern of dense features of a predetermined pitch and critical dimension.

And wherein the pattern of features is a template pattern of dense pillars.

Fritze et al. also teach that (col. 3, lines 20-29), FIG. 3 illustrates an example of a mask, (chromeless phase shift mask) having 180 degree phase region(s) 210 and a plurality of 0

degree phase regions 200, that can be used to exposed a substrate to realize a dense array of contact hole features. This mask, in this example, has a constant feature pitch of 250 nm.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 68-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fritze et al. (6,934,007) in view of Lee et al. (2002/0028541).

The claimed invention is directed to a method of forming a plurality of substantially evenly spaced pillars, the method comprising: forming a layer of a first material; depositing photoresist on the first material; patterning the photoresist using light having a wavelength of about 248 nm or more; etching the first material to form the plurality of substantially evenly spaced pillars, the pillars having a pitch between about 220 and about 280 nm.

And wherein the pitch is about 260 nm.

And wherein the pillars are portions of memory cells, that are a portion of a first memory level at a first height above a substrate.

And wherein the first memory level is in a monolithic three dimensional memory array comprising at least a second memory level formed at a second height above the substrate, the second height different from the first height.

Fritze et al. teach a method of forming a feature pattern on a substrate, comprising: (a) exposing the substrate, using a mask having a pattern of features thereon, with X-dipole illumination, to produce a dense feature illumination pattern on the substrate; (b) exposing the

substrate, using the same mask having the pattern of features thereon, with Y-dipole illumination, to produce a dense feature illumination pattern on the substrate; and (c) exposing the substrate to trim portions of the pattern on the substrate.

And wherein the pattern of features is a template pattern of regular dense features.

And wherein the pattern of features is a template pattern of dense features of a predetermined pitch and critical dimension.

And wherein the pattern of features is a template pattern of dense pillars.

Fritze et al. also teach that (col. 3, lines 20-29), FIG. 3 illustrates an example of a mask, (chromeless phase shift mask) having 180 degree phase region(s) 210 and a plurality of 0 degree phase regions 200, that can be used to exposed a substrate to realize a dense array of contact hole features. This mask, in this example, has a constant feature pitch of 250 nm.

The teachings of Fritze et al. differ from those of the applicant in that the applicant teaches that the pillars are portions of memory cells.

Lee et al. teach a memory comprising: a first pillar comprising a first contact, a body on said first contact, and a second contact on said body; a second pillar formed above said first pillar said second pillar comprising a third contact, a second body formed on said third contact and a fourth contact formed on said body; a first dielectric formed on the sidewalls of said first pillar and said second pillar; a nanocrystals film formed on and adjacent to said first dielectric adjacent to said first and second pillars; a second dielectric formed adjacent to said nanocrystals; a first control gate formed adjacent to said second dielectric adjacent to said first pillar; and a second control gate formed adjacent to said second dielectric adjacent to said second pillar.

For logic devices, in general, the size of the logic block is (x+1) sup2 times the cell area, where (x) is the number of inputs on the logic gate. Since the cell area here can be as small as 4F.sup.2, where F is the minimum feature size (half-pitch), then for F=0.25 microns, the minimum area per logic gate is 4(F(x+1)).sup.2, or 2.25 microns squared for a 2-input NAND or NOR gate. Preferably, the area per logic gate is 4(F(x+1)).sup.2 to 5(F(x+1)).sup.2 This size includes an "isolation" row and column on each edge of the block, that is shared with the next block.

It would have been obvious to one having ordinary skill in the art to take the teachings of Fritze et al. and combine them with the teachings of Lee et al. in order to make the claimed invention because a photolithography method for closer pillar formation would be desired as the use of photolithography is the conventional way of producing features for semiconductor devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
2/3/06